REMARKS

Claims 1 and 8 have been amended herein. Claims 1, 6-8, 12, and 13 remain pending. Claims 2-5, 9-11, and 14-20 have been withdrawn without prejudice in response to a restriction requirement. Applicant asserts that the amended claims of the present Application are patentable over the cited art.

35 USC Section 103 Rejections

Paragraphs 6-8 of the above referenced Office Action reject independent Claims 1 and 8 as being rendered obvious by Chisholm (U.S. Patent No. 5,968,143) in view of Wood (U.S. Patent No. 6,915,363) and in further view of Davis (U.S. Patent No. 6,298,407). Applicants respectfully traverse.

Independent Claims 1 and 8 have been amended to explicitly recite aspects regarding architecture of the bypass registers. For example, Claim 1 has been amended to recite a bypass register coupled to the bus master controller, wherein the bypass register is memory mapped and implements aggregation of transaction information from a host CPU by using a memory mapped data transfer. Applicants assert that these limitations are not shown by the cited references. Similar limitations are included in independent Claim 8.

In addition, Claims 1 and 8 further recite a bus master controller coupled to the disk I/O engine, a bypass register coupled to the bus master controller, an arbiter couple to the bus master controller and the disk I/O engine, to coordinate data transfers within the disk controller, and a device interface coupled to the disk I/O engine for interfacing the disk I/O. These claim limitations recite additional aspects of the architecture of the bypass registers and their functionality in control with respect to the disk I/O engine (e.g., Figure of the present application) for the Claim 1 embodiment. Applicants assert that these limitations are not shown by the cited references.

As recited in Claims 1 and 8, the bypass register is a memory mapped bypass register. Execution of a disk transaction are implemented by processing the disk transaction information from the memory mapped bypass register. Claim 1 further recites a disk controller for implementing efficient disk I/O for a computer system. The disk controller includes a bus interface for interfacing with a processor and a system memory of the computer system, a disk I/O engine coupled to the bus interface, and a device interface coupled to the disk I/O engine for interfacing the disk I/O engine with a disk drive. The disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command from the processor, the start up command configured to hide a start latency of the disk drive. The disk I/O

engine is further configured to execute a disk transaction by processing the disk transaction information from a memory mapped bypass register coupled to the disk I/O engine.

Accordingly, Claim 1 recites the disk I/O controller causing the startup of the disk drive upon receiving the command, enabling the disk controller to hide the start up latency of the disk drive, and processing this transaction information from a memory mapped bypass register. The bypass registers are memory mapped registers which functioned much faster than the prior art I/O mapped registers. Claim 8 has been amended to include similar limitations.

Applicants point out that Chisholm does not show the limitations regarding the architecture of the bypass registers. Chisholm does not show a bypass register coupled to the bus master controller, wherein the bypass register is memory mapped and implements aggregation of transaction information from a host CPU by using a memory mapped data transfer. Chisholm does not show a disk controller having a bus master controller coupled to the disk I/O engine, a bypass register coupled to the bus master controller, an arbiter couple to the bus master controller and the disk I/O engine, to coordinate data transfers within the disk controller, and a device interface coupled to the disk I/O engine for interfacing the disk I/O.

Chisholm is directed towards a general computer system that includes a general-purpose DMA controller. Applicant finds Chisholm to be directed towards the transfer of command blocks between a host processor and a local processor. Chisholm describes a system whereby a transfer signal is given to a command block transfer controller to start a command block transfer without a local processor unit intervention. Chisholm is relied upon to show the transferring of a command to a disk controller, wherein the command causes a start up of a disk drive coupled to the disk controller, as recited in Claim 1. As described above, Chisholm appears to be directed towards the transfer of command blocks between a host processor and a local processor. Chisholm describes a system whereby a transfer signal is given to a command block transfer controller to start a command block transfer without a local processor unit intervention.

There is no description within Chisholm of <u>a bus master controller</u> coupled to the disk I/O engine, <u>a bypass register coupled to the bus master controller</u>, <u>an arbiter couple to the bus master controller and the disk I/O engine</u>, to coordinate data transfers within the disk controller, and a device interface coupled to the disk I/O engine for interfacing the disk I/O. There is no description within Chisholm of any memory mapped registers or the use of such memory mapped registers to transfer a disk I/O commands. There is no description within Chisholm of the advantages of using memory mapped

bypass registers (e.g., as opposed to I/O mapped registers, etc.) for transferring disk commands.

The Wood reference is relied upon to show the transferring of a start command to an array of disk drives. The Davis reference is relied upon to show a bridge component of a computer system. Applicants point out that the addition of Wood and Davis does not cure the defect of Chisholm. Neither would nor Davis shows disk controller memory mapped bypass registers or the use of such memory mapped bypass registers to transfer a disk I/O command.

Accordingly, Applicant asserts that Chisholm, Wood and Davis combination does not render obvious the claimed invention within the meaning of 35 USC Section 103.

With respect to dependent Claim 6 and Claim 12, Claims 6 and 12 add further limitations to the disk controller, with respect to reciting a CPB pointer buffer coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers to extend to a number of disk transactions scheduled for execution by the disk I/O engine. These limitations are not shown or suggested by the cited references. The CPB pointer buffers are directly connected to the I/O engine for control in a manner independent of

the arbiter. Additionally, Claims 6 and 12 have been amended to explicitly recite the CPB pointer buffers directly connected to the disk I/O engine for control independent of the arbiter.

CONCLUSION

Applicant respectfully asserts that all remaining claims (e.g., Claims 1, 6-8, 12, and 13) are in condition for allowance and Applicant earnestly solicits such action from the Examiner. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: _May 28_, 2008

/Glenn Barnes/

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